IN THE CLAIMS

Please cancel claim 12, and amend claims 1-4, 13-17, and 20-22 as follows:

1. (CURRENTLY AMENDED) A device for generating at least one code phase, comprising

a shift register comprising N outputs and an input to which a code sequence is applied, N being an integer greater than two, the shift register being controlled by a clock signal; and

a plurality of phase delay networks, controlled by a separate clock signal distinct from the clock signal, each phase delay network comprising:

a plurality of multipliers, each multiplier receiving an input signal comprising a sequentially delayed code sequence and also receiving an input comprising a control signal; and

an adder block, coupled to the output of the plurality of multipliers, wherein the control signals are selected to allow only one of the sequentially delayed code sequence signals to reach the adder of each of the plurality of phase delay networks.

~~at least one logic branch, controlled by at least one combination control signal, on the basis of which the logic branch combines the code phase from i outputs of the shift register simultaneously, i being an integer between 2 and N, wherein said combination control signal is usable to set one or more weighting coefficients.~~

2. (CURRENTLY AMENDED) A device as claimed in claim 1, wherein at least one ~~logic branch~~ phase delay network comprises

i-two-input selectors, to the first input of each of which is connected one input of the shift register and to the second input is connected one combination control signal, and

an i-input combiner, to whose outputs are connected the outputs of said i selectors and from whose output said code phase is obtained.

3. (CURRENTLY AMENDED) A device as claimed in claim 1, wherein $N \geq (M1, M2)$, M1 and M2 being integers greater than one, and wherein the device comprises a first logic branch comprising M1 two-input selectors to which the outputs of M1 registers of the shift register and M1

combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an M1-input combiner to whose inputs are connected the outputs of said M1 selectors and from whose output the first code phase is obtained,

a second ~~logic branch~~ phase delay network comprising M2 two-input selectors to which the outputs of M2 registers of the shift register and M2 combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an M2-input combiner to whose inputs are connected the outputs of said M2 selectors and from whose output the second code phase is obtained.

4. (CURRENTLY AMENDED) A device as claimed in claim 3, wherein the device comprises a third ~~branch~~ phase delay network connected directly to the output of one register of the shift register and from which the third code phase is obtained.

5. (ORIGINAL) A device as claimed in claim 1, wherein i = N, and the device comprising

a first logic branch comprising N two-input selectors to which the outputs of the shift register and N combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an N-input combiner to whose inputs are connected the outputs of said N selectors and from whose output the first code phase is obtained,

a second logic branch comprising N two-input selectors to which the outputs of the shift register and N combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an N-input combiner to whose inputs are connected the outputs of said N selectors and from whose output the second code phase is obtained, and

a third logic branch comprising N two-input selectors to which the outputs of the shift register and N combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an N-input

combiner to whose inputs are connected the outputs of said N selectors and from whose output the third code phase is obtained.

6. (ORIGINAL) A device as claimed in claim 3, 4 or 5, wherein the first, second and third code phases obtained from the first, second and third logic branches, respectively, are an early, later and precise code phase, respectively.

7. (ORIGINAL) A device as claimed in claim 1, wherein N ≥(M1, M2, M3, M4), M1, M2, M3 and M4 being integers greater than one, and the device comprising

a first logic branch comprising M1 two-input selectors to which any M1 outputs of the shift register and any M1 combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an M1-input combiner to whose inputs are connected the outputs of said M1 selectors and from whose output the first code phase is obtained,

a second logic branch comprising M2 two-input selectors to which any M2 outputs of the shift register and M2 combination control signals are connected in such as way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an M2-input combiner to whose inputs are connected the outputs of said M2 selectors and from whose output the second code phase is obtained,

a third logic branch comprising M3 two-input selectors to which any M3 outputs of the shift register and M3 combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an M3-input combiner to whose inputs are connected the outputs of said M3 selectors and from whose output the third code phase is obtained, and

a fourth logic branch comprising M4 two-input selectors to which any M4 outputs of the shift register and M4 combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an M4-input combiner to whose inputs are connected the outputs of said M4 selectors and from whose output the fourth code phase is obtained.

8. (ORIGINAL) A device as claimed in claim 7, wherein the first, second, third and fourth code phases obtained from the first, second, third and fourth logic branches, are a first early code phase, a second early code phase, a first late code phase and a second late code phase, respectively.

9. (PREVIOUSLY PRESENTED) A device as claimed in anyone of claim 1 to 5 or 7 to 8, wherein the code phases obtained from the outputs of the logic branches are changed by software by changing the combination control signals.

10. (ORIGINAL) A device as claimed in claim 1, wherein the selectors are multipliers and/or AND gates.

11. (ORIGINAL) A device as claimed in claim 1, wherein the combiners are adders and/or OR gates.

12. (CANCELED)

13. (CURRENTLY AMENDED) A correlator comprising

generation means comprising a code generator for generating a local code, and a shift register, the shift register being controlled by a clock signal, the generation means generating at least one code phase from said local code, and

at least one correlator for correlating a signal applied to the correlator structure with said at least one locally generated code phase,

said generation means further comprising a plurality of phase delay networks, controlled by a separate clock signal distinct from the clock signal, each phase delay network comprising:

a plurality of multipliers, each multiplier receiving an input signal comprising a sequentially delayed code sequence and also receiving an input comprising a control signal; and

an adder block, coupled to the output of the plurality of multipliers, wherein the control signals are selected to allow only one of the sequentially delayed code sequence signals to reach the adder of each of the plurality of phase delay networks. ~~at least one logic branch controlled by at least one combination control signal, on the basis of which the logic branch combines the code phase from i~~

~~outputs of the shift register simultaneously, i being an integer between 2 and N, wherein said combination control signal is usable to set one or more weighting coefficients.~~

14. (CURRENTLY AMENDED) A correlator as claimed in claim 13, wherein at least one ~~logic branch~~ phase delay networks of said generation means comprises

i two-input selectors, to the first input of each of which is connected one input of the shift register and to the second input is connected one combination control signal, and

an i-input combiner, to whose outputs are connected the outputs of said i selectors and from whose output said code phase is obtained.

15. (CURRENTLY AMENDED) A correlator as claimed in claim 13 or 14, wherein the code phases obtained from the outputs of the ~~logic branch(es)~~ phase delay networks of said generation means are changed by software by changing the combination control signals.

16. (CURRENTLY AMENDED) A spread spectrum receiver for receiving a spread spectrum signal, the spread spectrum receiver comprising

generation means comprising a code generator for generating a local code, and a shift register, the generation means generating at least one code phase from said local code, and

at least one correlator for correlating a received spread spectrum signal with said at least one locally generated code phase,

said generation means further comprising ~~at least one logic branch controlled by at least one combination control signal, on the basis of which the logic branch combines the code phase from i outputs of the shift register simultaneously, i being an integer between 2 and N, wherein said combination control signal is usable to set one or more weighting coefficients.~~ a plurality of phase delay networks, controlled by a separate clock signal distinct from the clock signal, each phase delay network comprising:

a plurality of multipliers, each multiplier receiving an input signal comprising a sequentially delayed code sequence and also receiving an input comprising a control signal; and

an adder block, coupled to the output of the plurality of multipliers, wherein the control signals are selected to allow only one of the sequentially delayed code sequence signals to reach the adder of each of the plurality of phase delay networks.

17. (CURRENTLY AMENDED) A spread spectrum receiver as claimed in claim 16, wherein at least one ~~logic branch~~ phase delay network of said generation means comprises

i two-input selectors, to the first input of each of which is connected one input of the shift register and to the second input is connected one combination control signal, and

an i-input combiner, to whose outputs are connected the outputs of said i selectors and from whose output said code phase is obtained.

18. (ORIGINAL) A spread spectrum receiver as claimed in claim 16 or 17, wherein the code phases obtained from the outputs of the logic branch(es) of said generation means are changed by software by changing the combination control signals.

19. (ORIGINAL) A spread spectrum receiver as claimed in claim 16 or 17, wherein said code phase is phased spreading code replica.

20. (CURRENTLY AMENDED) The device of claim 1, wherein said one or more ~~weighting coefficients~~ control signals are applied to one or more of the i outputs of the shift register.

21. (CURRENTLY AMENDED) The device of claim 13, wherein said one or more ~~weighting coefficients~~ control signals are applied to one or more of the i outputs of the shift register.

22. (CURRENTLY AMENDED) The device of claim 16, wherein said one or more ~~weighting coefficients~~ control signals are applied to one or more of the i outputs of the shift register.